

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Schloesser, et al.

Attorney Docket: INF-135

Filed: February 13, 2004

Examiner: Andy Huynh

Serial No.: 10/777,128

Art Unit: 2818

For: Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

**FAX RECEIVED****APR 07 2006****OFFICE OF PETITIONS**

Mail Stop: Issue Fee  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Dear Sir:

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application. Copies of the U.S. Patents cited are not being submitted. However, Applicant has included a copy of the foreign patent.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(c)(1). Applicant hereby states that each item of information contained in this statement was first cited in a communication from a foreign patent office in a counterpart application not more than three months prior to the filing of this statement. As a result, no fee is due at this time.

Respectfully submitted,



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April 7, 2006

Date

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